Sheet 1 of 1

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO. TAM-103	SERIAL NO. 10/531287
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT T. TANIMOTO, et al.	
		FILING DATE April 14, 2005	GROUP

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
SP	AA	6,578,187	6/2003	YASUDA			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Abstract	
							Yes	No
SP	AM	10-149382	6/1998	JP			X	
SP	AN	2001-117855	4/2001				X	
	AO							
	AP							
	AQ							
	AR							
	AS							
	AT							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	~~AP~~	~~C-based Synthesis Experiences with a Behavior Synthesizer, "Cyber" Wakabayashi, et al.~~
	~~AQ~~	~~IEEE Std 1076, 2000 Edition. IEEE Standard VHDL Language Reference Manual.~~
SP	AR	Cycle-accurate RTL Modeling with Multi-Cycled and Pipelined Components, July 22, 2004.
SP	AS	HY-C LRM 1.2 Rev 1.1, Nov. 7, 2004
	~~AT~~	~~Kazutoshi Wakabayashi et al., "Densoyo LSI o Dosa"~~
	AU	Gosei de Kaihatsu, Kino Sekkei no Kikan ga 1/10 ni Tanshuku", Nikkei Electronics, Nikkei Business Publications, Inc., 12 February , 1996 (12.02.96), No. 6555, pages 147-169
	AV	Kurokawa, H. et al., "C++ Based System Simulator for Pre-Verification of System-on-a-Chip Devices", NEC Research & Development, 07 December, 2000 (07.12.00), Vol. 41, No.3, pages 258-263

No date/yr

No copies

Examiner	Date Considered
/Suchin Parihar/	09/14/2006